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REMARKS

Claims 1-32 are pending for examination with claims 1, 11, 21, and 31 being independent claims. Claim 32 has been added.

Rejections under 35 U.S.C. § 102

Claims 1-4, 6-7, 10-14, 16-17, 20-24, 26-27, and 30-31 stand rejected under 35 U.S.C. § 102 as being anticipated by Papaefsthatathiou et al., "An Introduction to the Layered Characterisation of High Performance Systems", Research Report CS-RR-335, The University of Warwick, December 5, 1997 [hereinafter Warwick]. Applicant respectfully traverses the rejection as follows.

In general, Warwick discloses a system for evaluating the performance of a single application in a parallel processing computer system, and in particular, the performance of a portion of the application, for example, programming subroutines that can be processed in a parallel processing environment. Warwick discloses "an application sub-task layer, which describes the sequential part of every sub-task within an application that can be executed in parallel" on page 2, paragraph 7, bullet 2. Also, Warwick requires an application object or model to evaluate the performance of the application in a parallel processing computer system. Warwick discloses, "a PACE program contains one application object", and further, "the object acts as the entry point of the performance study" on page 6, paragraph 3, lines 1-2.

Independent Claim 1

Claim 1 recites, *inter alia*, providing at least one hardware model, independently defined with regard to the workload specification. The Examiner suggests Warwick discloses providing at least one hardware model, independently defined with regard to the workload specification, comprising performance information by citing Warwick (page 2, paragraph 7, bullet 4). Applicant respectfully disagrees the hardware layer of Warwick discloses providing at least one hardware model, independently defined with regard to the workload specification.

The Warwick hardware layer is not independently defined with regard to the workload specification as recited in claim 1. Warwick recites "the characteristics and the parameters of a hardware object must be defined in a hardware symbol file", and further,

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"this file is included into the user defined objects that use hardware parameters" at page 5, paragraph 5, lines 3-5. The user defined objects of Warwick define the workload parameters. Thus, if the hardware object of Warwick is considered the hardware model of claim 1, the hardware object is not independently defined of the workload specification since it is compiled into the user defined objects which also include the workload parameters.

Alternatively, if the Examiner considers the hardware symbol file to be the hardware model of claim 1, the hardware symbol file is not functional within the system disclosed by Warwick. Specifically, the hardware symbol file is not functional until it has been compiled with the workload specification in the form of a hardware object.

The Examiner also suggests Warwick discloses providing a configuration defining system components and including a reference to the hardware model by citing Warwick (page 2, paragraph 7) as recited in claim 1. Applicant respectfully disagrees this cited section of Warwick teaches or suggests this feature of claim 1. The cited section of Warwick discloses "a parallel template layer, that describes the computation-communication pattern and other hardware resource usage" on page 2, paragraph 7. There is no recitation in this cited section of Warwick to a hardware model. Rather, the cited section of Warwick discloses that the parallel template layer "describes" "other hardware resource usage". A description of "other hardware resource usage" is not a reference to a hardware model.

Moreover, Warwick suggests the parallel template object includes no references to any other object including the hardware model. Warwick discloses "the syntax of the parallel template objects is similar to the application and subtask objects with the exception of the statement *link*" on page 8, paragraph 2. Further, Warwick discloses, "the purpose of the link statement is to modify external variables and options of the subtask objects and the hardware objects being used" on page 6, paragraph 2, list item 3, and "the *link* statement allows an object to modify the interface parameters and options of other objects" on page 13, paragraph 3. One skilled in the art would recognize that the link statement as a reference to subtask objects and hardware objects. Since the parallel template object excludes a link statement, Warwick specifically teaches away from the parallel template object including a reference to any other object, and in fact the lack of a

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reference to other objects or models is what distinguishes the parallel template object
from all other objects. Accordingly, the parallel template object as defined by Warwick
does not teach or suggest providing a configuration defining system components and
including a reference to the hardware model.

Thus, claim 1 patentably distinguishes over Warwick such that the rejection under
§ 102 should be withdrawn. Claims 2-4, 6-7, and 10 depend from claim 1, and for at
least the foregoing reasons are also patentable over Warwick.

Independent Claim 11

Claim 11 recites a performance technology infrastructure comprising a set of slots
for receiving a workload specification via the workload specification interface, and a
component configuration from the component configuration database, wherein hardware
model performance data corresponding to devices specifiable within the component
configuration is retrieved from at least one hardware model via the hardware model
interface. Applicant respectfully disagrees with the Examiner's suggestion that Warwick
at page 3, paragraph 2, teaches or suggests these features of claim 11. Rather, the cited
section discloses an evaluation engine. The evaluation engine of Warwick evaluates the
compiled PACE objects, and combines the results to produce detailed predictions of the
performance of the whole application (*See* page 9, paragraph 7). Assuming but not
agreeing the evaluation engine disclosed by Warwick in the cited section contains a set of
slots for receiving compiled PACE objects, these slots only accept compiled PACE
objects which are not a workload specification or a component configuration as recited in
claim 11. Warwick further discloses "the definition of hardware objects is not supported
directly by the PACE language" on page 5, paragraph 5, which further suggests that even
if PACE objects are assumed to fill slots in the evaluation engine by functionality, they
will not directly contain a workload specification or a component configuration as this is
not directly supported by the PACE language.

Further, Warwick neither discloses nor suggests a component configuration
database or a database of any type. Therefore, the component configuration recited in
claim 11 cannot be received from the component configuration database because this
database does not exist in Warwick. Assuming but not agreeing the component
configuration of Warwick is equivalent to the parallelization template and the component

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configuration stored therein is a component configuration database, the evaluation engine of Warwick does not receive this data directly in a slot. Rather, assuming but not agreeing the evaluation engine of Warwick contains a set of slots, the slots only accept compiled PACE objects and not the component configuration directly. Further, as stated above, the parallelization objects of Warwick do not directly contain a workload specification or a component configuration as this is not directly supported by the PACE language.

Thus, claim 11 patentably distinguishes over Warwick such that the rejection under § 102 should be withdrawn. Claims 12-14, 16-17, and 20 depend from claim 11, and for at least the foregoing reasons are also patentable over Warwick.

Independent Claim 21

Independent claim 21 is not anticipated by the cited sections of Warwick. As discussed above with respect to claim 1, Warwick does not teach or suggest providing at least one hardware model, independently defined with regard to the workload specification, comprising performance information. Claims 22-24, 26-27, and 30 depend from claim 21 and are also patentable over Warwick for the foregoing reasons.

Independent Claim 31

Independent claim 31 is not anticipated by the cited sections of Warwick. Warwick does not teach or suggest a set of slots for receiving a workload specification via the workload specification interface, and a component configuration from the component configuration database, wherein hardware model performance data corresponding to devices specifiable within the component configuration is retrieved from at least one hardware model via the hardware model interface, similar to the argument presented with respect to claim 21.

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Rejections under 35 U.S.C. § 103

Claims 5, 15, 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Warwick, in view of U.S. Patent 6,748,569 B1 to Brooke (hereinafter Brooke). Applicant respectfully traverses the rejection as follows.

Claims 5, 15, and 25 depend from independent claims 1, 11, and 21 respectively and are patentable for at least the same reasons set forth above.

Claims 8, 18, and 28 stand rejected under 35 U.S.C. § 103 as being unpatentable over Warwick, in view of Papaefstathious et al., "A Common Workload Interface for the Performance Prediction of High Performance Systems", IEEE Int. Symp. On Computer Architecture, Workshop on Performance Analysis in Design (PAID'98) June 1998 (hereinafter PAID'98).

Claims 8, 18, and 28 depend from independent claims 1, 11, and 21 respectively and are patentable for at least the same reasons set forth above.

Claims 9, 19, and 29 stand rejected under 35 U.S.C. § 103 as being unpatentable over Warwick, in view of Brooke and PAID'98.

Claims 9, 19, and 29 depend from independent claims 1, 11, and 21 respectively and are patentable for at least the same reasons set forth above.

New Claim 32

New claim 32 depends from independent claim 1 and is patentable for at least the foregoing reasons. Moreover, claim 32 recites, *inter alia*, a method for computer system analysis where in the computer system is a networked computer environment. As noted above, Warwick is directed towards performance analysis of a single application. As defined by the Applicant in the Specification at page 4, lines 4-6, "the infrastructure and method provide a flexible platform for carrying out analysis of various computer networks under various workload conditions".

Since the analysis of the performance of a single application in a parallel network is not analysis of a networked computer environment, claim 32 is not anticipated or rendered obvious by Warwick.

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CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, please charge any deficiency to **Deposit Account No. 50-0463.**

Respectfully submitted,
Papaefstathiou., Applicant

By:
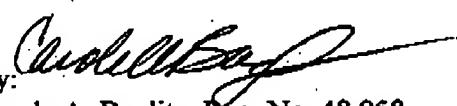
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bec. 22, 2004

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